M5M467405J,TP -5,-6,-7

HYPER PAGE MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 16777216-word by 4-bit dynamic RAMS, fabricated with the high performance CMOS process,and is ideal for large-capacity memory systems where high speed, low power dissipation , and low costs are essential.
The use of double-layer aluminum process combined with triple-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M467405XX-5	50	13	25	13	84	340
M5M467405XX-6	60	15	30	15	104	300
M5M467405XX-7	70	20	35	20	124	250

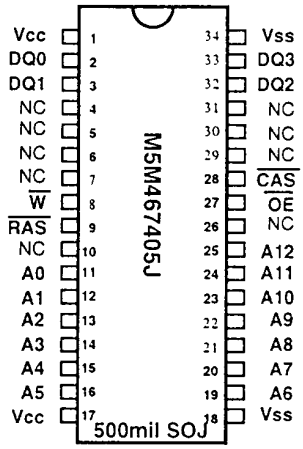
XX=J,TP

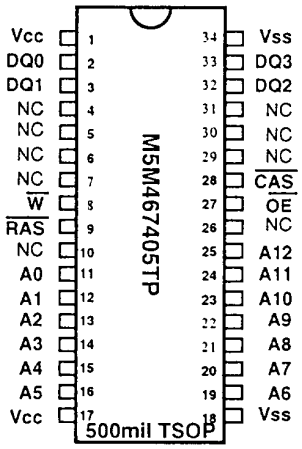
- Standard 34 pin SOJ, 34 pin TSOP
- Single 3.3 ± 0.3V supply
- Low stand-by power dissipation
  1.8mW (Max) ..... LVCMOS input level
- Low operating power dissipation
  M5M467405xx-5 ..... 414.0mW (Max)
  M5M467405xx-6 ..... 378.0mW (Max)
  M5M467405xx-7 ..... 324.0mW (Max)
- Hyper-page mode , Read-modify-write,
  $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write mode, $\overline{OE}$ and $\overline{W}$ to control output buffer impedance
- All inputs, output LVTTL compatible and low capacitance
- 4096 refresh cycles every 64ms

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)





PIN DESCRIPTION

Pin Name	Function
A_0-A_{12}	Address Inputs
DQ0-DQ3	Data Inputs / Outputs
$\overline{RAS}$	Row Address Strobe Input
$\overline{CAS}$	Column Address Strobe Input
$\overline{W}$	Write Control Input
$\overline{OE}$	Output Enable Input
Vcc	Power Supply (+3.3V)
Vss	Ground (0V)
NC	No Connection

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FUNCTION

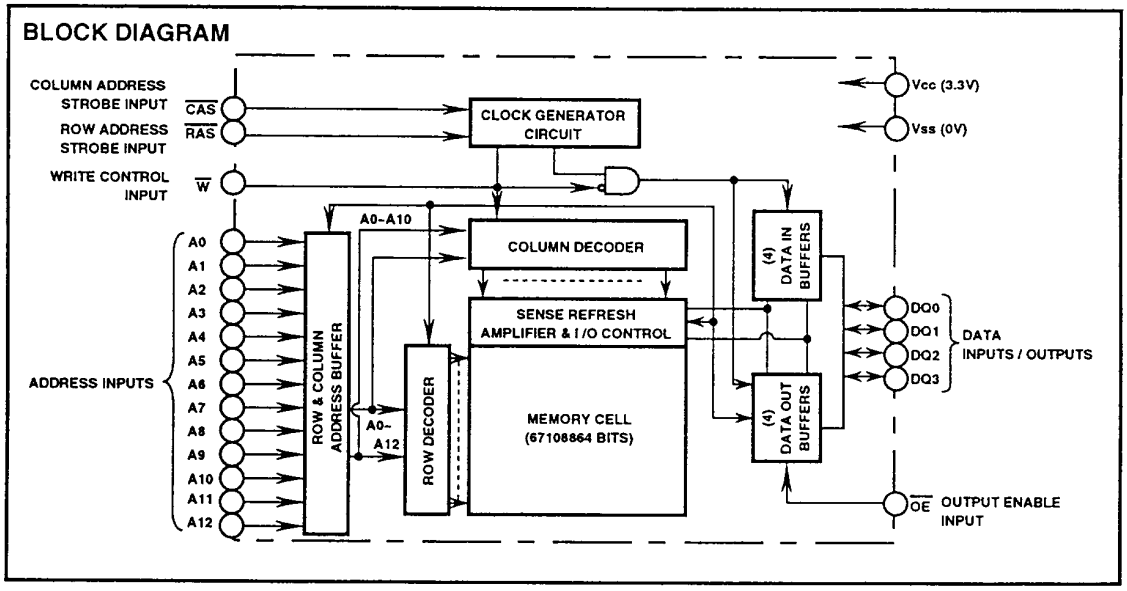
The M5M467405J, TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., hyper page mode, $\overline{CAS}$ before RAS refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	NO	Hyper page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	NO	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	NO	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	NO	
Hidden refresh	ACT	ACT	DNC	ACT	DNC	DNC	OPN	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid,APD : applied, OPN : open

BLOCK DIAGRAM



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HYPER PAGE MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	-0.5 ~ 4.6	V
VI	Input voltage		-0.5 ~ Vcc+0.5	V
VO	Output voltage		-0.5 ~ Vcc+0.5	V
IO	Output current		50	mA
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0 ~ 70	°C
Tstg	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0 ~ 70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	3.0	3.3	3.6	V
Vss	Supply voltage	0	0	0	V
VIH	High-level input voltage, all inputs	2.0		Vcc+0.3	V
VIL	Low-level input voltage, all inputs	-0.3		0.8	V

Note 1 : All voltage values are with respect to Vss

ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70°C, Vcc=3.3± 0.3V, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
VOH	High-level output voltage		IOH=-2mA	2.4		Vcc	V
VOL	Low-level output voltage		IOL=2mA	0		0.4	V
IOZ	Off-state output current		Q floating 0V≦VOUT≦Vcc	-10		10	μA
II	Input current		0V≦VIN≦Vcc+0.3V, Other inputs pins=0V	-10		10	μA
ICC1 (AV)	Average supply current from Vcc operating (Note 3,4,5)	M5M467405-5	$\overline{RAS}$, $\overline{CAS}$ cycling tRC=tWC=min. output open			115	mA
		M5M467405-6				105	
		M5M467405-7				90	
ICC2	Supply current from Vcc , stand-by		$\overline{RAS}$= $\overline{CAS}$ =VIH, output open			1	mA
			$\overline{RAS}$= $\overline{CAS}$≧Vcc -0.2,output open			0.5	
ICC4(AV)	Average supply current from Vcc Hyper-Page-Mode (Note 3,4,5)	M5M467405-5	$\overline{RAS}$=VIL, $\overline{CAS}$ cycling tPC=min. output open			135	mA
		M5M467405-6				120	
		M5M467405-7				110	
ICC6(AV)	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M467405-5	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling tRC=min. output open			155	mA
		M5M467405-6				130	
		M5M467405-7				110	

Note 2: Current flowing into an IC is positive, out is negative.
3: Icc1 (AV), Icc4 (AV) and Icc6 (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: Icc1 (AV) and Icc4 (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column Address can be changed once or less while $\overline{RAS}$=VIL and $\overline{CAS}$=VIH.

CAPACITANCE (Ta=0 ~ 70°C, Vcc=3.3± 0.3V, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
CI (A)	Input capacitance,address inputs	VI=Vss f=1MHz Vi=25mVrms			5	pF
CI ($\overline{OE}$)	Input capacitance, $\overline{OE}$ input				7	pF
CI ($\overline{W}$)	Input capacitance, write control input				7	pF
CI ($\overline{RAS}$)	Input capacitance, $\overline{RAS}$ input				7	pF
CI ($\overline{CAS}$)	Input capacitance, $\overline{CAS}$ input				7	pF
CI/O	Input/Output capacitance, data ports				7	pF

SWITCHING CHARACTERISTICS (Ta=0~ 70°C, Vcc=3.3± 0.3V, Vss=0V, unless otherwise noted , see notes 6,14,15)

Symbol	Parameter		Limits						Unit
			M5M467405-5		M5M467405-6		M5M467405-7		
			Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note 7,8)		13		15		20	ns
tRAC	Access time from $\overline{RAS}$	(Note 7,9)		50		60		70	ns
tAA	Column address access time	(Note 7,10)		25		30		35	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 7,11)		30		35		40	ns
tOEA	Access time from $\overline{OE}$	(Note 7)		13		15		20	ns
tOHC	Output hold time from $\overline{CAS}$		5		5		5		ns
tOHR	Output hold time from $\overline{RAS}$	(Note 13)	5		5		5		ns
tCLZ	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
tOEZ	Output disable time after $\overline{OE}$ high	(Note 12)		13		15		20	ns
tWEZ	Output disable time after $\overline{WE}$ high	(Note 12)		13		15		20	ns
tOFF	Output disable time after CAS high	(Note 12,13)		13		15		20	ns
tREZ	Output disable time after $\overline{RAS}$ high	(Note 12,13)		13		15		20	ns

Note 6: An initial pause of 500 μ s is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{CAS}$ before $\overline{RAS}$ refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods (greater than 64 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to 1TTL loads and 50pF,VOH=2.4V(IOH=-2mA) and VOL=0.4V(IOL=-2mA).
The reference levels for measuring of output signals are 2.0V(VOH) and 0.8V(VOL).

8: Assumes that $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$ and $t_{CP} \geqq t_{CP(max)}$.

9: Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10: Assumes that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.

11: Assumes that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

12: $t_{OEZ\,(max)}$,$t_{WEZ(max)}$,$t_{OFF(max)}$ and $t_{REZ(max)}$defines the time at which the output achieves the high impedance state ($I_{OUT} \leqq I \pm 10$ μ A I) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

13: Output is disabled after both $\overline{RAS}$ and $\overline{CAS}$ go to high.